APPLICATION		REVISION			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	C65	1	PRELIMINARY RELEASE	1-31-91	

1.0 DESCRIPTION

This specification describes the requirements FOR a custom DMA Gate array IC used in the C65. It functions as a DMA controller with a few tricks up its sleeve, hence, DMAgic.

Specifically, special features include:

* List-based fetching of DMA command sequences.
* Ability to CHAIN multiple DMA command sequences.
* Absolute Address access to entire System Memory.
* Blocks can be up to 64 K bytes long.
* Windowed Block capability using MODulus function.
* DMAgic operations yield to VIC video and eXternal DMA accesses.
* DMAgic operations can optionally yield to system interrupts.
* Interrupted DMAgic operations can be continued/resumed, or cancelled.
* Data ReQuest handshaking support for IO devices.
* Independent memory/mapped IO selection for source and destination.
* Independent memory tranfer DIRection for source and destination.
* Independent MODulus enable for source and destination.
* Independent HOLD (fixed pointer) for source and destination.

1.1 CONFIGURATION

This device shall be configured in a standard 48-pin dual in-line package (DIP).

1.2 SOURCES

Refer to Approved Vendor List for sources.

COMMODORE P. N.	STATUS				
390957-01	ACTIVE				
390957-02	ACTIVE				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/- 0.02
3 PLACE DECIMALS +/- 0.010

DRAWN	Mike Rivers	DATE
SYSTEM ENG.		DATE
TEST ENG		DATE
COMP. ENG	Drew Shannon	DATE
CIRCUIT ENG.		DATE

Commodore
1200 WILSON DRIVE
WEST CHESTER, PA. 19380
(215) 431-9100

TITLE:
IC, DMAgic, GATE ARRAY,4151 F018

SIZE A | DRAWING NUMBER 390957

SCALE | SHEET 1 OF 5

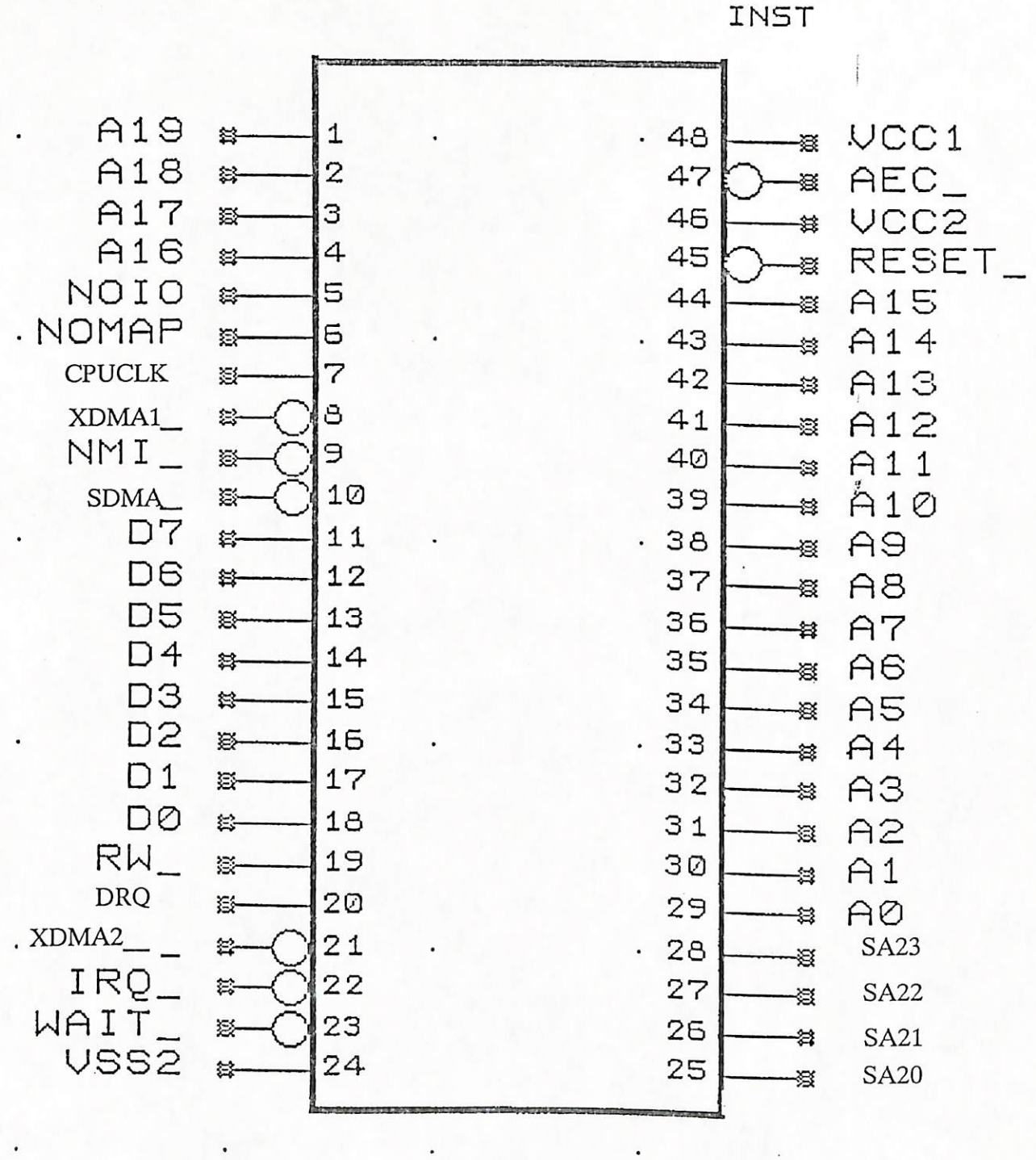
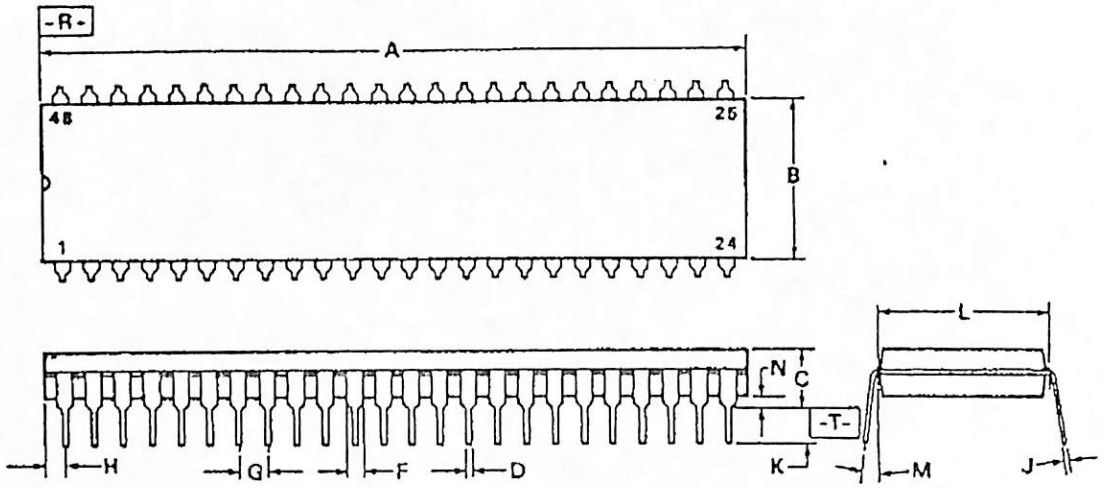


FIGURE 1
DMAgic PINOUT

Commodore	TITLE: IC, DMAgic, GATE ARRAY,4151 F018			
SIZE	DRAWING NUMBER: 390957	REV.: 1	SCALE	SHEET 2 OF 5



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	61.34	62.10	2.415	2.445
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.55	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.79 BSC		0.070 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.42	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:

1. -R- IS END OF PACKAGE DATUM PLANE. -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 1 AND 48:
   ⌖ | 0.51 (0.020) | T | B Ⓜ | A
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ | 0.25 (0.010) | T | B Ⓜ
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: INCH.

FIGURE 2
PACKAGE DIMENSIONS

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1.3 APPLICABLE DOCUMENTS

Commodore Engineering Policy 1.02.007 Integrated Circuit Qualification Procedure
Commodore Engineering Policy 1.02.008 Integrated Circuit Process Test Specification

2.0 PIN DESCRIPTIONS

NAME	PIN	DIRECTION	DESCRIPTION
CPUCLK	7	IN	Main system clock (1 or 3.5 MHz)
RESET	45	IN	System Reset
NOIO	5	IN	Select signal for memory-mapped IO
AEC*	47	IN	Request for video DMA
XDMA1*	8	IN	Request for eXternal DMA #1
XDMA2*	21	IN	Request for eXternal DMA #2
IRQ*	22	IN	Standard Interrupt Request
NMI*	9	IN	Non-maskable Interrupt request
DRQ	20	IN	Data request handshake signal
WAIT*	23	OUT	When low, indicates that DMA is spin-waiting
MAP*	6	OUT	Select signal for MAPPER memory or IO memory
SDMA*	10	OUT	System DMAagic bus request
SA23-20	28-25	OUT	System-Chunk address bits
A19-16	1-4	I/O	System-Bank address bits
A15-0	44-29	I/O	4510 standard address bus
D7-0	11-18	I/O	System data bus
RW*	19	I/O	System Read/Write line

3.0 PHYSICAL REQUIREMENTS

3.1 MARKING

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code. Pin No. 1 shall be identified.

3.2 PACKAGING

The interconnected logic circuitry shall be contained in a standard, plastic ZIP (Zig-Zag in-line package) Package with exterior dimensions per Figure 2.

4.0 ENVIRONMENTAL REQUIREMENTS

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request):

Operating Temperature	0 to 70 deg. C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85 deg. C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

4.1 PROCESS QUALIFICATION TESTS

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

4.2 ENVIRONMENTAL TEST CONDITIONS

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85 deg. C and 95% RH non-condensing) for 168 hours.
2. Operating life (1000 hours at 70 deg. C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120 deg. C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883,Method 2015, using water and trichloroethane
6. Solder temperature resistance (250 deg. C for five seconds)
7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

4.3 MINIMUM ACCEPTANCE LEVEL

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

4.4 AGE OF DEVICES

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

APPROVED VENDOR LIST

This sheet must be removed from this document before the document is shown or transmitted to a vendor.

Commodore Part Number	Vendor	Vendor Part Number
390957-01	CSG	4151 F018
390957-02	CSG	4151 F018A

Commodore			TITLE: IC, DMAgic, GATE ARRAY,4151 F018	
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